REMARKS

The present response is to the Office Action mailed in the above-referenced case on September 24, 2003. Claims 1-12 are standing for examination. The Examiner has objected to the disclosure, the drawings and to claims 1, 3, 5-7, 9, 11 and 12 due to informalities. Claim 4 is rejected under 35 U.S.C. 112, second paragraph as being indefinite. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Emer (U.S. 6,4700,443 B1), hereinafter Emer.

Applicant has carefully studied the prior art presented by the Examiner, and the Examiner's objections, rejections and statements of the instant Office Action. In response, applicant herein amends the specification and claims to overcome the Examiner's objections due to informalities, and 112 rejection of claim 4. Regarding the merit rejections of applicant's claims, applicant herein presents argument to more particular point out the subject matter regarded as the invention, and to establish that the claims as amended distinguish unarguably over the prior art presented by the Examiner. Applicant points out and argues the key limitations in the base claims that the Examiner appears to have misunderstood or overlooked in his rejections and statements.

The Examiner has objected to the disclosure, stating that the headings of each section should not be underlined or in boldface type as described in 37 CFR 1.77(c), and the word "and" is consecutively repeated on page 5, line 16, and the title of the invention is not descriptive. In response, applicant herein amends the headings of the sections of the disclosure in accordance with the Examiner's suggestion, amends the text to delete the repeated word, and amends the title of

the invention to more clearly indicate the invention to which the claims are directed.

Regarding the Examiner's objection to drawings, applicant's Fig. 3 shows a connection between the fetch program counters (FPC 37) and select logic 35, which has a cross strike but does not show a number to indicate the bus width of the connection. The connection, however, may be of various types, such as a serial or parallel bus connection, twisted pair, digital wire line or wireless connection, or some other connection type. Accordingly, applicant herein provides a proposed drawing correction removing the cross strike from the connection in question.

Regarding the Examiner's objection to claim 1, applicant herein amends the claim to overcome the objection. For convenience, applicant reproduces claim 1 as amended below.

Applicant's claim 1 as amended now recites:

1. (Currently Amended) A pipelined multistreaming processor, comprising:

an instruction source;

a plurality of streams enabled to fetch instructions at different times from the instruction source;

a dispatch stage for selecting and dispatching instructions to a set of execution units;

a set of instruction queues having one queue associated with each stream in the plurality of streams, and located in the pipeline between the instruction source and the dispatch stage; and

a select system for selecting streams in each cycle to fetch instructions from the instruction source wherein the select system selects a number of streams

for which to fetch instructions, which are fewer in number than the number of streams in the plurality of streams.

Regarding the Examiner's objection to claims 3 and 9, the phrase of both claims in question recites "...according to the to the program counters." In response applicant herein amends the language of both claims to correct the duplicated portion of the phrase.

Regarding the Examiner's objection to claim 5, the claim recites a limitation which is duplicated from claim 1. Accordingly, applicant herein cancels claim 5.

Claim 6 is objected to because the claim recites the acronym "ALU", which is correctly used for the phrase "Arithmetic-Logic Units", while claim 12 and portions of the specification use the abbreviation "ALS". In order to correct the inconsistencies and overcome the Examiner's objection, applicant herein amends claim 12 and portions of the specification to recite the correct acronym "ALU"

The Examiner has objected to method claim 7, stating that, in step (a), it is unclear if the recitation "instruction queue" is replacing the previously mentioned one or if it is a separate entity, and that the phrase "decoupling" is unclear as used in the context of the language of the claim. In response, applicant herein amends the language of the claim to replace the word "decoupling" with "disassociating" in the preamble, and further to replace the second mentioned phrase "instruction queue" in step (a) with "instruction source".

Regarding the Examiner's objection to claims 11 and 12, applicant herein amends claim 11 to correct the antecedent basis.

The Examiner has rejected claim 4 as being indefinite, stating that there is no antecedent basis for the phrase "the instruction cache". In response, applicant

herein amends the language of claim to replace the phrase " the instruction cache" with "the instruction source".

The Examiner has rejected claims 1-12 on the merits as being anticipated by Emer. Regarding claim 1, the Examiner has stated that the Emer discloses all of applicant's claimed limitations, including a set of instruction queues associated with each stream in the plurality of streams, and located in the pipeline between the instruction source and the dispatch stage. The Examiner has further stated that Emer (col. 6, lines 24-27) teaches that instructions can be fetched and then stored in a buffer, and further teaches (col. 4, lines 8-9) Emer discloses an embodiment where a distinct fetch unit is included for each thread, and therefore, there exists a queue for each fetch unit and thus one queue for each stream.

Applicant respectfully traverses the Examiner's statement, and points out to the Examiner that the fact that Emer teaches multiple fetch units does not require that there also be separate multiple instruction queues. Emer does not teach separate instruction queues. The Examiner's reasoning is based on supposition, and the instruction queue disclosed by Emer clearly and unarguably cannot read on applicant's limitation recited in claim 1, of "a set of instruction queues having one queue associated with each stream in the plurality of streams".

Emer teaches separate fetch units, but clearly does not teach or suggest a plurality of separate instruction queues as taught in applicant's invention and recited in applicant's claims. Referring to Examiner now to Fig. 2 of Emer, and the supporting text disclosure of the specification, Emer discloses (col. 4, line 16 - col. 5, line 1) that "Once the instructions from the different threads are redefined to operate on distinct physical registers, the instructions from different threads are combined into a single instruction queue 30". A single instruction queue 30 is provided in this embodiment, however, Emer discloses that both an integer and floating point instruction queue may also be provided, but as argued above by

applicant, the teaching clearly cannot read on applicant's claimed limitation of a set of instruction queues having one queue associated with each stream in the plurality of streams.

Applicant's claimed set of instruction queues is a key and patentable distinction over the reference of Emer. This advantageously distinct aspect of applicant's invention enables monitoring of the instruction queues separately, for the number of instructions in each instruction queue of the plurality of instruction queues, providing for efficient load balancing, as well as several other advantages over the prior art, as described below.

Referring the Examiner now to applicant's specification, with particular reference to Fig. 3, the unique and novel set of instruction queues 39 provides decoupling, or disassociation, of the dispatch stage from the fetch stage in the pipeline. Due to applicant's multiple instruction queues 39, the dispatch stage has a larger pool of instructions from which to select to dispatch to execution units, and the efficiency of dispatch is therefore greatly improved, as the number of instructions that may be dispatched per cycle is maximized. This structure and operation allows a large number of streams of a DMS processor to execute instructions continually while permitting the fetch mechanism to fetch from a smaller number of streams in each cycle. Fetching from a smaller number of streams is important because the hardware and logic necessary to provide additional ports into the instruction cache is significant. As an added benefit, unified access to a single cache is provided. The unique instruction queue architecture of applicant's teaching allows fetched instructions to be buffered after fetch and before dispatch, and the instruction queue read mechanism allows the head of the queue to be presented to dispatch in each cycle, allowing a variable number of instructions to be dispatched from each stream in each cycle. With this multiple instruction queue arrangement, one can take advantage of instruction

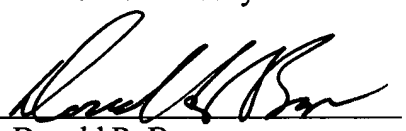
stream locality, while maximizing the efficiency of the fetch mechanism in the presence of stalls and branches. By providing a fetch mechanism that can support up to eight instructions from two streams, one can keep the instruction queues full while not having to replicate the fetch bandwidth across all streams.

In view of the facts and substantial arguments presented above by applicant on behalf of claim 1, applicant strongly believes that claim 1, as judicially amended to overcome the Examiner's objection to the claim due to informalities, is clearly and unarguably patentable over the prior art of Emer cited and applied by the Examiner. Independent claim 7 is applicant's method claim in accordance with the limitations of claim 1, and the Examiner has rejected claim 7 using the same criteria as applied to claim 1 above. Claim 7 has also been slightly amended to overcome the Examiner's objection to the claim due to informalities. Claim 7 as amended also specifically recites, in step (a), the key and patentable limitation, as argued above on behalf of claim 1, of a set of instruction queues, one instruction queue for each stream, in the pipeline between the instruction source and the dispatch stage. Therefore, claim 7 is also clearly and unarguably patentable over the prior art, as the reference provided by the Examiner in no way anticipates the limitation as taught in applicant's invention. Many of the depending claims have been herein amended by applicant to overcome the Examiner's objections due to informalities, and rejection for indefiniteness. Depending claims 2-6 and 8-12 are then patentable on their own merits, or at least as depended from a patentable claim.

It is therefore respectfully requested that this application be reconsidered, the claims be allowed, and that this case be passed quickly to issue. If there are any time extensions needed beyond any extension specifically requested with this amendment, such extension of time is hereby requested. If there are any fees due

beyond any fees paid with this amendment, authorization is given to deduct such fees from deposit account 50-0534.

Respectfully Submitted,
Mario Nemirovsky et al.

by 
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